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| 10/019,437 | 12/31/2001 | Yasuyuki Doi | 60188-124 | 4255 |

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| EXAMINER | |
|---|---|
| NELSON, ALECIA DIANE | |
| **ART UNIT** | **PAPER NUMBER** |
| 2675 | |

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/019,437 | DOI ET AL. | |
| | Examiner | Art Unit | |
| | Alecia D. Nelson | 2675 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *9-14 and 18-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-14* is/are allowed.

6)☒ Claim(s) *18-21,23,24,26 and 27* is/are rejected.

7)☒ Claim(s) *22,25 and 28-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. ***Claims 18 and 19*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. (U.S. Patent No. 6,211,849).

With reference to **claims 18 and 19**, Sasaki et al. teaches a liquid crystal driving circuit (23) for driving a liquid crystal element (22) in which a plurality of source driver circuit devices (1) having an input side pad unit (2) and an output side pad unit (3) arranged on a liquid crystal panel, the liquid crystal driving circuit comprising a reference voltage production circuit (2) capable of producing a plurality of reference

voltages to drive the plurality of source driver circuit devices (see column 4, lines 3-18), and a reference voltage wire unit capable of receiving the plurality of reference voltages and providing the plurality of reference voltages to the plurality of source driver circuit device (connecting from circuit 25 to the source driver circuits), the reference voltage wire unit including a plurality of in-chip reference voltage wire units (leading from input-side to output-side), each in-chip reference voltage wire unit being configured in each source driver circuit device of the plurality of source driver circuit devices, and including a plurality of in-chip reference voltage wires, each in-chip reference voltage wire connecting each input-side pad to the output side pad unit (see Figure 4), and a plurality of inter-chip reference voltage wire units (10), each inter-chip reference voltage wire unit being configured between any two adjacent source driver circuit devices of the plurality of source driver circuit devices and including a plurality of inter-chip reference voltage wires, each inter-chip reference voltage wire connecting each output side pad of one source driver circuit device of the two adjacent source driver circuit devices to each input-side pad of the other source driver circuit device of the two adjacent source driver circuit devices (see Figure 3).

While Sasaki et al. teaches the usage of the input side pad and the output side pad, there fails to be any disclosure towards the side pads being composed of a plurality of input-side pads or output-side pads. However, it would have been obvious to one having ordinary skill in the art to allow for such an arrangement to be used in the device as taught by Sasaki et al. thereby providing each of the signal lines (CLK, DATA, CNT) to have separate input side pads as well as output side pads.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for a device similar to that which is taught by Sasaki et al. wherein the input side pads and the output side pads of the source drivers are composed of a plurality of individual side pads for each of the signal lines in order to thereby provide a driver IC arrangement that has increased transmission without increasing the dimensions of the frame region.

3. ***Claims 20 and 21*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. as applied to claim 18 above, and further in view of Applicant's admitted prior art (APA).

With reference to **claim 20**, Sasaki et al. teaches that the driving circuit (1) includes a plurality of in-chip reference voltage wires (10) extending from one end to the other end of the source driver circuit for supplying a plurality of reference voltages different from one another (see Figure 3). Sasaki et al. also teaches that various power voltages are input to the driver (1) via the power input (11) and supplied to circuit components such as the buffer amplifiers (4, 8) and other circuitry and are output to the next driver IC (see column 7, lines 6-15)

The admitted prior art teaches the usage of two branch reference voltage wires (131) branching off from a corresponding in-chip reference voltage wire of the plurality of in-chip reference voltage wires, and a selection circuit (134) for selecting a voltage for driving the liquid crystal element (see Figure 10).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the usage of the branch reference voltage wires and a selection circuit as disclosed by the admitted prior art in the driver circuits which allow for in-chip wiring in the display device similar to that which is taught by Sasaki in order to thereby reduce the required wiring area for signal transmission in order to produce higher resolution for larger screen sizes without increasing the dimensions of the frame region of the display.

With reference to **claim 21**, Sasaki et al. fails to teach that the semiconductor integrated circuit device further includes a subdivided voltage production circuit wherein the selection circuit selects on of the subdivided voltages.

The admitted prior art teaches the limitations of claim 4, including the subdivided voltage production circuit (132) and the selection circuit (134) (see pages 5-6).

Therefore it would have been obvious to on having ordinary skill in the art to allow the device of Sasaki et al. to include the subdivided voltage production circuit and the selection circuit as taught by admitted prior art in order to generate voltage signals for controlling the brightness of light passing through the liquid crystal element when driving the liquid crystal display panel thereby producing higher resolution for larger screen sizes without increasing the dimensions of the frame region.

4. ***Claims 23, 24, 26, and 27*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. in view of Kawaguchi et al. (U.S. Patent No. 5, 670,994) and APA.

With reference to **claim 23**, Sasaki et al. teaches a semiconductor integrated circuit device (1) provided in a liquid crystal module (22) having a liquid crystal element, the semiconductor integrated circuit comprising an input-side pad unit (2) receiving a plurality of reference voltages, output-side pad unit (3) outputting the plurality of reference voltages (see column 4, lines 3-18), a in-chip reference voltage wire unit (leading from input side to output side), and a plurality of buffer amplifiers (4, 8) receiving a reference voltage and thereafter supplying an output voltage (see column 7, lines 6-15).

While teaching the usage of the input and output pad unit there fails to be any disclosure towards the side pads being composed of a plurality of input-side pads or output-side pads. However, it would have been obvious to one having ordinary skill in the art to allow for such an arrangement to be used in the device as taught by Sasaki et al. thereby providing each of the signal lines (CLK, DATA, CNT) to have separate input side pads as well as output side pads. Further, Sasaki et al. fails to teach that the in-chip reference voltage wires directly connect the input side pad unit to the output side pad unit to transmit the plurality of reference voltages, a plurality of branch reference voltage wires branching of from the in-chip reference voltage wire, or a selection circuit for selecting a voltage for driving the liquid crystal element from the output voltages of the buffers.

Kawaguchi et al. teaches a liquid crystal panel (20) having liquid crystals (21) having flexible wiring boards (4) having drive ICs (5) for driving the liquid crystal panel, wherein the flexible wiring boards (230) containing a connecting line (256) for connecting the input terminal (245) directly to the output terminal (247), while a branch line (257) is formed for connecting the connecting line (256) to its corresponding electrode bump (252) of the IC (229) (see column 29, lines 38-49).

The admitted prior art teaches the usage of two branch reference voltage wires (131) branching off from a corresponding in-chip reference voltage wire, and a selection circuit (134) for selecting a voltage for driving the liquid crystal element (see Figure 10).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of the direct connection of the input terminals to the output terminals and the branch wires, as taught by Kawaguchi et al., and the selection circuit as disclosed by the APA in the driver circuits similar to that which is taught by Sasaki et al. which would thereby allow the driver ICs of the liquid crystal module to have the ability to transfer directly to the output so that some signals input from the input terminals can be transferred to another adjacent IC. This prevents degrading the signals as it is being transferred and reduces the required wiring area for signal transmission in order to produce higher resolution for larger screen sizes.

With reference to **claim 24**, Sasaki et al. fails to teach that the semiconductor integrated circuit device further includes a subdivided voltage production circuit wherein the selection circuit selects on of the subdivided voltages.

The admitted prior art teaches the limitations of claim 4, including the subdivided voltage production circuit (132) and the selection circuit (134) (see pages 5-6).

Therefore it would have been obvious to on having ordinary skill in the art to allow the device of Sasaki et al. to include the subdivided voltage production circuit and the selection circuit as taught by admitted prior art in order to generate voltage signals for controlling the brightness of light passing through the liquid crystal element when driving the liquid crystal display panel thereby producing higher resolution for larger screen sizes without increasing the dimensions of the frame region.

With reference to **claim 26**, Sasaki et al. teaches the input side pad (2) is configured along one side of the integrated circuit and the output side pad (3) is configured along another side of the integrated circuit (see Figure 3).

With reference to **claim 27**, Sasaki et al. fails to teach that the buffer has an offset canceling function capable of reducing a potential difference between the input voltage and the output voltage.

Kawaguchi et al. teaches a chip capacitor containing within the flexible wiring boards (230) for signal adjustment being connected to the connecting lines (256, 253). Thereby any differences in display grade among the ICs of the flexible wiring boards are reduced (see column 29, lines 50-54).

### *Allowable Subject Matter*

5. ***Claims 22, 25, and 28-30*** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Response to Arguments*

6. Applicant's arguments with respect to ***claims18-30*** have been considered but are moot in view of the new ground(s) of rejection.

In response to the Applicant's concerns about the IDS statements filed December 31, 2001 and May 7, 2001, the Examiner request that the applicant resend the list to the IDS statements to alleviate any confusion.

### *Conclusion*

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703) 305-0143. The examiner can normally be reached on Monday-Friday 9:30-6:00. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

adn/ADN
September 17, 2004

AMR A. AWAD
PRIMARY EXAMINER